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**Form PTO-1449** (modified)  
List of Patents and Publications  
For Applicant's Information  
Disclosure Statement  
(Use several sheets if necessary)

ATTY. DKT. NO. 5181-68300  
APPLICANT: Lee  
FILING DATE: January 4, 2001

SERIAL NO. 09/755,479  
GROUP: 2155

**U.S. PATENT DOCUMENTS**

EXAM. INITIALS	REF. DES.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
<i>mm</i>	D1	6,128,277	10/3/00	Bruck, et al.	—	—	
<i>mm</i>	D2	5,612,897	3/18/97	Rege	—	—	

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**FOREIGN PATENT DOCUMENTS**

EXAM. INITIALS	REF. DES.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO
<i>mm</i>	D3	00/14932	3/16/00	WO	—	—	

**OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)**

<i>mm</i>	D4	G. Albertengo, et al., "Optimal Routing Algorithms for Bidirectional Manhattan Street Network," IEEE, 1991, 3 pages.

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7-20-04

Information Disclosure Statement--PTO 1449 (modified)

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2155**U.S. PATENT DOCUMENTS**

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<i>mjw</i>	A1	6,016,510	1/18/00	Quattromani, et al.	—	—	
<i>mjw</i>	A2	6,023,753	2/8/00	Pechanek, et al.	—	—	
<i>mjw</i>	A3	5,689,661	11/18/97	Hayashi, et al.	—		
<i>mjw</i>	A4	6,167,502	12/26/00	Pechanek, et al.	—		
<i>mjw</i>	A5	6,101,181	8/8/00	Passint, et al.	—		
<i>mjw</i>	A6	5,720,025	2/17/98	Wilkes, et al.	—		
<i>mjw</i>	A7	5,970,232	10/19/99	Passint, et al.	—		
<i>mjw</i>	A8	6,055,618	4/25/00	Thorson	—		
<i>mjw</i>	A9	5,701,416	12/23/97	Thorson, et al.	—		
<i>mjw</i>	A10	5,737,628	4/7/98	Birritella, et al.	—		
<i>mjw</i>	A11	5,689,646	11/18/97	Thorson	—		
<i>mjw</i>							

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**FOREIGN PATENT DOCUMENTS**

EXAM. INITIALS	REF. DES.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO
<i>mjw</i>	A12	99/26429	5/27/99	WO	—	—	
<i>mjw</i>	A13	0 785 512	7/23/97	EP	—	—	

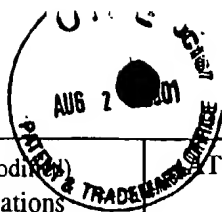
**OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)**

<i>mjw</i>	A14	Bradley Kuzmaul, Mercury Computer Systems, Inc., "The RACE Network Architecture," (posted at www.mc.com/techlit/#tech_brief prior to this), 6 pages.
<i>mjw</i>	A15	R.Y. Wang, T.E. Anderson and D.A. Patterson, "Virtual Log Based File Systems For a Programmable Disk," Proc. Third Symposium on Operating Systems Design and Implementation, February 1999 (Also appeared as University of California Technical Report CSD-98-1031, 16 pages.
<i>mjw</i>	A16	Prasant Mohapatra, "Wormhole Routing Techniques for Directly Connected Multicomputer Systems, ACM Computing Surveys, Vol. 30, No. 3, September 1998, 37 pages.
<i>mjw</i>	A17	Christopher Glass and Lionel Ni, "The Turn Model for Adaptive Routing," Journal of the Association for Computing Machinery, Vol. 41, No. 5, September 1994, pp. 874-902.

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<b>Form PTO-1449</b> (modified) List of Patents and Publications For Applicant's Information Disclosure Statement (Use several sheets if necessary)		PATENT & TRADEMARK OFFICE CITY. DKT. NO. 5181-68300 APPLICANT: Lee FILING DATE: January 4, 2001	SERIAL NO. 09/755,479 GROUP: <del>2151</del> 2155 <b>RECEIVED</b>
<b>OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)</b> AUG 27 2001			
<i>mul</i>	A18	Reddy, Dept. of Computer & Information Sciences, "A Dynamically Reconfigurable WDM LAN Based on Reconfigurable Circulant Graph," IEEE, 1996, 4 pages. <b>Technology Center 2100</b>	
<i>mul</i>	A19	Various Abstracts beginning with Funahashi, Jouraku and Amano, "Adaptive Routing for Recursive Diagonal Torus," Transactions of the Institute of Electronics, Information and Communication Engineers D-I, vol. J83D-I, no. 11, November 2000, pp. 1143-53.	
<i>mul</i>	A20	Milan Kovacevic, Center for Telecommunications Research, "On Torus Topologies with Random Extra Links," IEEE 1996, pp. 410-418.	
<i>mul</i>	A21	Dally, et al., The Torus Routing Chip, Distributed Computing, Springer-Verlag 1986, pp. 187-196.	
<i>mul</i>	A22	Susan Hinrichs, "A Compile Time Model for Composing Parallel Programs," IEEE Parallel and Distributed Technology, 1995, 19 pages.	
<i>mul</i>	A23	"CRAY T3D System Architecture Overview Manual," <a href="ftp://ftp.cray.com/product-info/mpp/T3D_Architecture_Over/T3D.overview.html">ftp://ftp.cray.com/product-info/mpp/T3D_Architecture_Over/T3D.overview.html</a> , Cray Research, 1993, 40 pages.	
<i>mul</i>	A24	Marco Fillo, et al., "The M-Machine Multicomputer," Laboratory for Computer Science, Massachusetts Institute of Technology, A.I. Memo No. 1532, Ann Arbor, March 1995, 14 pages.	
<i>mul</i>	A25	Noakes, et al., "The J-Machine Multicomputer: An Architectural Evaluation," Proceedings of the 20 <sup>th</sup> International Symposium on Computer Architecture, May 1993, 12 pages.	
<i>mul</i>	A26	Dally, et al., "Architecture of a Message-Driven Processor," International Conference on Computer Architecture, June 1987, pp. 189-196.	
<i>mul</i>	A27	Dennison, Lee and Dally, "High-Performance Bidirectional Signalling in VLSI," Massachusetts Institute of Technology, October 12, 1992, 20 pages.	
<i>mul</i>	A28	Dally, et al., "Architecture and Implementation of the Reliable Router," Mass. Institute of Technology, Proceedings of Hot Interconnects II, Stanford CA, August 1994, 12 pages.	
<i>mul</i>	A29	Dally, et al., "The Reliable Router: A Reliable and High-Performance Communication Substrate for Parallel Computers," Proceedings of the First International Parallel Computer Routing and Communication Workshop, Seattle WA, May 1994, 15 pages.	
<i>mul</i>	A30	Dennison, et al., "Low-Latency Plesiochronous Data Retiming," Mass. Institute of Technology, Proceedings of the 1995 Advanced Research in VLSI Conference, Chapel Hill NC, March 1995, 12 pages	
<i>mul</i>	A31	Whay S. Lee, "Mechanism for Efficient, Protected Messaging," Massachusetts Institute of Technology, Dept. of Electrical Engineering and Computer Science, January 20, 1999, 147 pages.	
<i>mul</i>	A32	Dennison, "Reliable Interconnect Networks for Parallel Computers," Mass. Institute of Technology, Dept. of Electrical Engineering and Computer Science, April 18, 1991, 79 pages.	
<i>mul</i>	A33	Thucydides Xanthopoulos, "Fault Tolerant Adaptive Routing in Multicomputer Networks," Dept. of Electrical Engineering and Computer Science, Mass. Institute of Technology, January 20, 1995, 152 pages.	
<i>mul</i>	A34	Dennison, "The Reliable Router: An Architecture for Fault Tolerant Interconnect," Dept. of Electrical Engineering and Computer Science, Mass Institute of Technology, May 24, 1996, 145 pages.	

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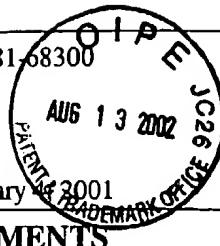
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EXAM. INITIALS	REF. DES.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
<i>mw</i>	B1	5,612,897	3/18/97	Rege	—	—	
<i>mw</i>	B6	5,862,312	1/19/99	Mann, et al.	—	—	

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**FOREIGN PATENT DOCUMENTS**

EXAM. INITIALS	REF. DES.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO
<i>mw</i>	B2	669 584	2/20/95	EP	—	—	
<i>mw</i>	B3	550 853	12/16/92	EP	—	—	
<i>mw</i>	B4	99/63442	12/9/99	WO	—	—	
<i>mw</i>	B5	646 858	8/26/94	EP	—	—	
<i>mw</i>	B2	669 584	2/20/95	EP	—	—	
<i>mw</i>	B7	99/17217	4/8/99	WO	—	—	
<i>mw</i>	B8	94/12939	6/9/94	WO	—	—	
<i>mw</i>	B9	439 693	8/7/91	EP	—	—	
<i>mw</i>	B10	92/06436	4/16/92	WO	—	—	

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